Claims

What is claimed is:

[c1] A method for providing verification for a simulation design, comprising:

obtaining the simulation design comprising a programming language interface system call;

encoding a target of the programming language interface system call into the simulation design to obtain a first modified simulation design;

modifying the programming language interface system call to reference the target in the first modified simulation design to obtain a second modified simulation design; and

verifying the second modified simulation design using a simulation testbench.

[c2] The method of claim 1, wherein the simulation design comprises a register transfer level design.

[c3] The method of claim 1, wherein encoding the target of the programming language interface comprises:

obtaining a set of hardware state elements from the simulation design;

obtaining a set of high-level state elements from a high-level design;

determining a common set of state elements from the set of hardware state elements and the set of high-level state elements;

identifying at least one relationship between the high-level state element and the hardware state element in the common set of state elements;

determining whether the at least one relationship is influenced by a test vector to obtain an influenced set of relationships; and

encoding the influenced set of relationships to obtain a modified simulation design.

[c4] The method of claim 3, wherein encoding the influenced set of relationships comprises:

obtaining high-level state element values for the high-level state elements in the influenced set of relationships from a simulation of the high-level design; and

storing the high-level state element values in an array.

[c5] The method of claim 4, wherein the high-level state element values are obtained during concurrent execution of a high-level design simulation and verification of the second modified hardware-level design.

[c6] The method of claim 3, wherein the hardware state element comprises at least one from the group consisting of a processor register and a memory.

[c7] The method of claim 3, wherein the high-level state element comprises at least one from the group consisting of a flip-flop, a latch, and a memory.

[c8] The method of claim 3, wherein the relationship comprises at least one of the group consisting of a one-to-one relationship, a one-to-many relationship, and a relationship defined by a mathematical function.

[c9] The method of claim 1, wherein the second modified hardware-level design is verified on a hardware-based simulation test bench.

[c10] A computer system for providing verification for a simulation design, comprising:

a processor;

a memory;

a storage device; and

software instructions stored in the memory for enabling the computer system to perform:

obtaining the simulation design comprising a programming language interface system call;

encoding a target of the programming language interface system call into the simulation design to obtain a first modified simulation design;

modifying the programming language interface system call to reference the target in the first modified simulation design to obtain a second modified simulation design; and

verifying the second modified simulation design using a test vector.

[c11] The computer system of claim 10, wherein the simulation design comprises a resistor transfer level design.

[c12] The computer system of claim, 10, wherein encoding the target of the programming language interface comprises:

obtaining a set of hardware state elements from the simulation design;

obtaining a set of high-level state elements from a high-level design;

determining a common set of state elements from the set of hardware state elements and the set of high-level state elements;

identifying at least one relationship between the high-level state element and the hardware state element in the common set of state elements;

determining whether the at least one relationship is influenced by the test vector to obtain an influenced set of relationships; and

encoding the influenced set of relationships to obtain a modified simulation design.

[c13] The computer system of claim 12, wherein encoding the influenced set of relationships comprises:

obtaining high-level state element values for the high-level state elements in the influenced set of relationships from a simulation of the high-level design; and

storing the high-level state element values in an array.

[c14] The computer system of claim 12, wherein the high-level state element values are obtained during concurrent execution of a high-level design simulation and verification of the second modified hardware-level design.

[c15] The computer system of claim 12, wherein the hardware state element comprises at least one from the group consisting of a processor register and a memory.

[c16] The computer system of claim 12, wherein the high-level state element comprises at least one from the group consisting of a flip-flop, a latch, and a memory.

[c17] The computer system of claim 12, wherein the relationship comprises at least one of the group consisting of a one-to-one relationship, a one-to-many relationship and a relationship defined by a mathematical function.

[c18] The computer system of claim 10, wherein the second modified hardware-level design is verified on a hardware-based simulation test bench.

[c19] A system for verifying a simulation design, comprising:

a simulation design comprising a component, an encoded target of a programming language interface system call, and a reference to the encoded target;

a test vector providing an input signal value for the component in the simulation design; and

a simulation testbench providing functionality to verify the simulation design using the test vector.

[c20] Apparatus providing verification for a simulation design, comprising:

means for obtaining the simulation design comprising a programming language interface system call;

means for encoding a target of the programming language interface system call into the simulation design to obtain a first modified simulation design;

means for modifying the programming language interface system call to reference the target in the first modified simulation design to obtain a second modified simulation design; and

means for verifying the second modified simulation design using a test vector.